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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,505	02/27/2004	Jae-Yoel Kim	678-1362	9103

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EXAMINER	
ALIA, CURTIS A	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,505	KIM ET AL.	
	Examiner	Art Unit	
	Curtis A. Alia	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment filed 25 April 2008 has been entered. No claims have been added, amended or cancelled.

Response to Arguments

1. Applicant's arguments filed 25 April 2008 have been fully considered but they are moot in view of new grounds of rejection.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re*

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 9-10, 12-15 and 17-18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 32-35 of copending Application No. 09/879,688 (hereafter "Kim"). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons outlined blow.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claim 9, Kim discloses an apparatus comprising a bi-orthogonal sequence generator for generating a bi-orthogonal sequence by performing an AND operation between bits of physical layer header information bits and predetermined basis Walsh code sequences (see claim 32, an orthogonal sequence generator for creating a plurality of bi-orthogonal

sequences…selected from bi-orthogonal sequences by first information bits, claim 35, multipliers (AND) multiplying second information part with basis orthogonal sequence, claim 33, base orthogonal sequences include Walsh codes), a mask sequence generator for generating a mask sequence by performing an AND operation between less significant bits of the physical layer header information bits and predetermined mask sequences (see claim 32, a mask sequence generator for creating a plurality of mask sequences…selected from mask sequences by second information bits, claim 35, multipliers (AND) multiplying third information part with mask sequences) and an exclusive OR element for performing an exclusive OR operation on a symbol-by-symbol basis between the bi-orthogonal sequence output from the bi-orthogonal sequence generator and the mask sequence output from the mask sequence generator, so as to output a single encoded symbol sequence (see claim 8, an adder for adding bi-orthogonal sequence from the orthogonal sequence generator and a mask sequence from the mask sequence generator).

While the claims of copending application to Kim do not explicitly teach that the AND operation is performed between the more significant bits and Walsh code sequence and the AND operation is performed between the less significant bits and mask sequences, it would have been obvious to one having ordinary skill in the art at the time the invention was made to perform these AND operations on any part of a string of bits, since it has been held that rearranging parts of an invention involves only routine skill in the art.

Regarding claim 10, Kim does not explicitly disclose that the physical layer header information bits are 11 bits in length, but it would have been obvious to a person having ordinary skill in the art at the time of the invention as a design choice use 11 bits of the header, since such

a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 12, Kim discloses a bit "1" generator for generating a sequence of 1s (see claim 32, 1-bit generator for generating same symbols), a basis Walsh code generator (see claim 33, Walsh codes) and a plurality of AND elements for receiving all bits of the information as their inputs (see claim 35, multipliers (AND)), performing respective AND operations between a first information part bits and the basis Walsh code sequences, and performing an AND operation between another bit and the sequence of 1s (see claim 32, the bi-orthogonal sequence is generated by combination (multiplying) the orthogonal sequence with the same symbols (1s)).

Kim does not explicitly teach that the Walsh code generator generates exactly 5 basis Walsh code sequences of length 32 or that the AND operations are being performed on 11 bits and 5 Walsh code sequences and 5 mask sequences. However, it would have been an obvious matter of design choice to a person having ordinary skill in the art at the time the invention was made to perform the AND operations on 11 bits of information, and to divide the AND operations (5 bits, 1 bit, 5 bits) between the Walsh codes and the mask sequences, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 13, Kim discloses a basis mask sequence generator for generating basis mask sequences (see claim 32, mask sequence generator generates sequences of length m), and a

plurality of AND elements for receiving all bits of the physical layer header information as their inputs (see claim 32, a plurality of multipliers (AND)), and performing respective AND operations between some bits of the bits and the basis mask sequences (see claim 32, multiplying the sequences by third information part).

Kim does not explicitly teach that the basis mask sequence generator generates exactly 5 basis mask sequences of length 32, and the AND operation is on 11 bits, and the AND operation between the 5 mask sequences is with 5 less significant bits of the information. However, it would have been an obvious matter of design choice to a person having ordinary skill in the art at the time of the invention to perform AND operation between a number of mask sequences (5) of length 32 (m) with a number of the information bits (5) of the 11 (k) bits of the information bits, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 14, Kim discloses a method comprising generating a bi-orthogonal sequence by performing an AND operation between first bits of information bits and predetermined basis Walsh code sequences (see claim 32, orthogonal sequence generator, multiplying the first sequence by associated bits, claim 32, bi-orthogonal sequences are generated from the orthogonal sequences), generating a mask sequence by performing an AND operation between second information bits of the information bits and predetermined mask sequences (see claim 32, mask sequence generator, multiplier for multiplying the mask sequence with third information part), performing an exclusive OR operation on a symbol-by-symbol basis between the generated bi-orthogonal sequence and the generated mask sequence (see claim 35,

an adder for adding the multiplied sequences to output a symbol sequence), and outputting a single encoded symbol sequence (see claim 35, outputting a symbol sequence).

Kim does not explicitly teach that the bits are less significant bits and more significant bits. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to perform these AND operations on any part of a string of bits, since it has been held that rearranging parts of an invention involves only routine skill in the art.

Regarding claim 15, Kim does not explicitly disclose that the physical layer header information bits are 11 bits in length, but it would have been obvious to a person having ordinary skill in the art at the time of the invention as a design choice use 11 bits of the header, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 17, Kim discloses generating a sequence of 1s (see claim 32, 1-bit generator for generating same symbols (1s), generating basis Walsh code sequences (see claim 32, orthogonal sequence generator, claim 33, Walsh code sequences), performing respective AND operations between first bits of the bits and the basis Walsh code sequences (see claim 35, multipliers multiplying second information part with orthogonal sequences) and performing an AND operation between a bit of the bits and the sequence of 1s (see claim 35, combining the first information part with the same symbol sequence (1s)).

Kim does not explicitly disclose that the information is 11 bits in length, or that 5 basis Walsh code and 5 mask sequences are generated, or that more significant bits and less significant

bits are multiplied to respective Walsh code and mask sequences. However, it would have been an obvious matter of design choice to a person having ordinary skill in the art at the time of the invention to perform AND operation between a number of mask sequences (5) of length 32 (m) with a number of the information bits (5) of the 11 (k) bits of the information bits, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 18, Kim discloses generating 5 basis mask sequences of length 32; b-2) receiving, as inputs, all bits of the physical layer header information (see claim 32, mask sequence generator generates sequences of length m) and performing respective AND operations between bits of the bits and the basis mask sequences (see claim 32, multiplying the sequences by third information part).

Kim does not explicitly teach that the basis mask sequence generator generates exactly 5 basis mask sequences of length 32, and the AND operation is on 11 bits, and the AND operation between the 5 mask sequences is with 5 less significant bits of the information. However, it would have been an obvious matter of design choice to a person having ordinary skill in the art at the time of the invention to perform AND operation between a number of mask sequences (5) of length 32 (m) with a number of the information bits (5) of the 11 (k) bits of the information bits, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

4. Claims 11 and 16 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 32-35 of copending Application No. 09/879,688 in view of IEEE 802.17.

This is a provisional obviousness-type double patenting rejection.

Regarding claim 11, Kim does not explicitly teach that the physical layer header information bits include information of a MAC frame's transfer rate and information of a payload length.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by IEEE 802.17. In particular, IEEE teaches that the physical layer header information bits include information of a MAC frame's information of a payload length (see Figure 1.1 and sections 1.1.1-1.2.2, MAC frame format in IEEE 802.17 defines a field in the MAC frame header indicating the length of the frame, which can be used to further determine the length of the payload using the payload type field).

In view of the above, having the apparatus of Kim, then given the well-established teaching of IEEE, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of Kim as taught by IEEE, since IEEE 802.17 is the standard for MAC frame structure.

Regarding claim 16, Kim does not explicitly teach that the physical layer header information bits include information of a MAC frame's transfer rate and information of a payload length.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by IEEE 802.17. In particular, IEEE teaches that the physical layer header information bits include information of a MAC frame's information of a payload length (see Figure 1.1 and sections 1.1.1-1.2.2, MAC frame format in IEEE 802.17 defines a field in the MAC frame header indicating the length of the frame, which can be used to further determine the length of the payload using the payload type field).

In view of the above, having the apparatus of Kim, then given the well-established teaching of IEEE, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of Kim as taught by IEEE, since IEEE 802.17 is the standard for MAC frame structure.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 9-10, 12-15 and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (newly cited US 2002/0013926).

Regarding claim 9, Kim discloses an apparatus for encoding physical layer header information (see paragraph 6, TFCI is an indicator field used in a dedicated physical data channel's data frame to inform a receiver of the frame transfer rate of the current service frame) comprising a bi-orthogonal sequence generator (see paragraph 18, bi-orthogonal sequence is generated by performing an operation on orthogonal sequences) for generating a bi-orthogonal sequence by performing an AND operation between less significant bits of physical layer header information bits and predetermined Walsh code sequences (see paragraph 64, each Walsh code sequence is multiplied (AND operation) with a corresponding information bit), a mask sequence generator for generating a mask sequence by performing an AND operation between more significant bits of the physical layer header information bits and predetermined mask sequences (see paragraph 65, each mask sequence is multiplied (AND operation) with a corresponding information bit), and an exclusive OR element for performing an exclusive OR operation on a symbol-by-symbol basis between the bi-orthogonal sequence output from the bi-orthogonal sequence generator, so as to output a single encoded symbol sequence (see paragraph 66, an adder performs an XOR operation on the symbol outputs from the multipliers of the Walsh code sequences, the 1-bit sequence, and the mask sequences to a single sequence of symbols).

Note: Kim teaches generating the bi-orthogonal sequences using the less significant bits and generating the mask sequences using the more significant bits of the input information bits; whereas the instant application claims that the bi-orthogonal sequences are generated using the

more significant bits and the mask sequences are generated using the less significant bits. Inverting the bit significance does not define a patentably distinct invention over that in the system of Kim. The inversion of the bit encoding operation presents no new or unexpected results, so long as the information bits are encoded using all of the prescribed steps claimed and the encoding is performed with success. Therefore, to have the bi-orthogonal sequence generated from the more significant bits and the mask sequence generated from the less significant bits, as opposed to the inverse, would have been routine experimentation and optimization in the absence of criticality.

Regarding claim 10, Kim discloses that the physical layer header information bits are 11 bits in length (see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI).

Regarding claim 12, Kim discloses that the bi-orthogonal sequence generator comprises a bit "1" generator for generating a sequence of 1s (see paragraph 18, lines 1-2, a one-bit generator generates bits having 1s), a basis Walsh code generator for generating 5 basis Walsh code sequences of length 32 (see paragraph 63, Walsh codes W1, W2, W4, W8, W16 and W32 are all length 64, also see paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus can increase the number of Walsh codes needed for the encoding, also see paragraph 11, the encoding can be performed on 32-bit sequences, such as (32,10)) and a plurality of AND elements for receiving all 11 bits of the physical layer header information as their inputs (see figure 7, multipliers 740-745 are AND elements, also see

paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI), performing respective AND operations between the less significant bits of the 11 bits and the 5 basis Walsh code sequences (see figure 7, a5-a0 are all multiplied with the Walsh code sequences W1, W2, W4, W8, W16, and W32, respectively, also see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI), and performing an AND operation between one bit of the 11 bits and the sequence of 1s (see figure 7, multiplier 746 performs an AND operation between the sequence of 1s from the 1-bit generator 700 and input bit a6).

Regarding claim 13, Kim discloses that the mask sequence generator comprises a basis mask sequence generator for generating 5 basis mask sequences of length 32 (see paragraph 20, mask sequences are generated having length 48, also see paragraph 11, the encoder can encode based on 32-bit sequences such as (32,10), also see paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus increase the number of mask sequences needed for the encoding to 5), and a plurality of AND elements for receiving all 11 bits of the physical layer header information as their inputs (see figure 7, multipliers 740-749), and performing respective AND operations between 5 more significant bits of the 11 bits and the 5 basis mask sequences (see figure 7, AND operation between M1 and a7, M2 and a8, and M4 and a9, also see paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus can increase the number of mask sequences needed for the encoding to 5).

Regarding claim 14, Kim discloses a method comprising generating a bi-orthogonal sequence by performing an AND operation between more significant bits of physical layer header information bits and predetermined basis Walsh code sequences (see figure 7, multipliers 740-745 are AND elements), generating a mask sequence by performing an AND operation between less significant bits of the physical layer header information bits and predetermined mask sequences (see figure 7, a5-a0 are all multiplied with the Walsh code sequences W1, W2, W4, W8, W16, and W32, respectively), performing an exclusive OR operation on a symbol-by-symbol basis between the generated bi-orthogonal sequence and the generated mask sequence and outputting a single encoded symbol sequence (see paragraph 66, an adder performs an XOR operation on the symbol outputs from the multipliers of the Walsh code sequences and the mask sequences to a single sequence of symbols).

Regarding claim 15, Kim discloses that the physical layer header information bits are 11 bits in length (see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI).

Regarding claim 17, Kim discloses that step a) comprises that the steps of generating a sequence of 1s (see paragraph 18, lines 1-2, a one-bit generator generates bits having 1s), generating 5 basis Walsh code sequences of length 32 (see paragraph 63, Walsh codes W1, W2, W4, W8, W16 and W32 are all length 64, also see paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus can change the number of

Walsh codes needed for the encoding to 5, also see paragraph 11, the encoding can be performed on 32-bit sequences, such as (32,10)), receiving, as inputs, all 11 bits of the physical layer header information (see figure 7, multipliers 740-745 are AND elements, also see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI), performing respective AND operations between 5 more significant bits of the 11 bits and the 5 basis Walsh code sequences (see figure 7, a5-a0 are all multiplied with the Walsh code sequences W1, W2, W4, W8, W16, and W32, respectively, also see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI) and performing an AND operation between a sixth bit of the 11 bits and the sequence of 1s (see figure 7, multiplier 746 performs an AND operation between the sequence of 1s from the 1-bit generator 700 and input bit a6).

Regarding claim 18, Kim discloses that the step b) comprises the steps of generating 5 basis mask sequences of length 32 (see paragraph 20, mask sequences are generated having length 48, also see paragraph 11, the encoder can encode based on 32-bit sequences such as (32,10), also see paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus increase the number of mask sequences needed for the encoding to 5), receiving, as inputs, all 11 bits of the physical layer header information (see figure 7, multipliers 740-749, also see paragraph 17, the TFCI encoding method can be performed on k number of bits, meaning that this process can be performed on an 11 bit TFCI) and performing respective AND operations between 5 less significant bits of the 11 bits and the 5 basis mask sequences (see figure 7, AND operation between M1 and a7, M2 and a8, and M4 and a9, also see

paragraph 96, lines 8-12, the encoder can adapt the encoding based on the number of information bits, thus can increase the number of mask sequences needed for the encoding to 5).

Claim Rejections - 35 USC § 103

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of IEEE 802.17 (previously cited).

Regarding claim 11, Kim discloses that the physical layer header information (TFCI field) bits include information of the frame's transfer rate (see column 1, lines 32-37), but does not explicitly teach that the transfer rate is of a MAC frame, or that the information of the payload length is disclosed.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by IEEE 802.17. In particular, IEEE teaches that the physical layer header information bits include information of a MAC frame's information of a payload length (see Figure 1.1 and sections 1.1.1-1.2.2, MAC frame format in IEEE 802.17 defines a field in the MAC frame header indicating the length of the frame, which can be used to further determine the length of the payload using the payload type field).

In view of the above, having the apparatus of Kim, then given the well-established teaching of IEEE, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of Kim as taught by IEEE, since IEEE 802.17 is the standard for MAC frame structure.

Regarding claim 16, Kim discloses that the physical layer header information (TFCI field) bits include information of the frame's transfer rate (see column 1, lines 32-37), but does not explicitly teach that the transfer rate is of a MAC frame, or that the information of the payload length is disclosed.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by IEEE 802.17. In particular, IEEE teaches that the physical layer header information bits include information of a MAC frame's information of a payload length (see Figure 1.1 and sections 1.1.1-1.2.2, MAC frame format in IEEE 802.17 defines a field in the MAC frame header indicating the length of the frame, which can be used to further determine the length of the payload using the payload type field).

In view of the above, having the method of Kim, then given the well-established teaching of IEEE, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of Kim as taught by IEEE, since IEEE 802.17 is the standard for MAC frame structure.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis A. Alia whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2616

/Curtis A Alia/
Examiner, Art Unit 2616
7/14/2008

CAA